ABSTRACT OF THE DISCLOSURE

A multi-processor system apparatus allows a compiler to perform a static scheduling action easily and can conduct the transfer of data packets without collision in response to a common pattern of simultaneous access demands. Processor elements are interconnected by a multi-stage interconnection network having multiple stages. As each of switching elements in the multi-stage interconnection network is preliminarily subjected to the static scheduling action of a compiler. The multi-stage interconnection network is emulated without producing collision of data. When the transfer of packets is carried out in one clos network arrangement of the multi-stage interconnection network, the scheduling of switching elements SE0 to SE3 in the exchanger at Level 1 is determined so that a packet lost in the arbitration is transferred through the free port of any applicable one of the switching elements.